REMARKS

The Examiner objected to the specification as failing to provide antecedent basis for the claimed subject matter relating to a "digital domain" and "RF."

Turning first to "digital domain," Applicants point out that the application as originally filed used the phrase "digital domain" in originally filed claims 11 and 28. Applicants would further point out that the phrase "digital domain" is well known and understood by those skilled in the art to refer to processing operations performed by digital circuitry, such the digital tuners and decoders disclosed in the specification. Paragraphs 7, 36, 41, 73, and 74 of the specification further refer to a "digital part" which Applicants would assert supports the claimed "digital domain" language and would be understood as such by one skilled in the art. Applicants present an amendment to the specification to provide explicit support for "digital domain". If the Examiner wishes, Applicants would accept an Examiner's amendment to replace "digital domain" in the claim language with "digital part."

Turning next to "RF," Applicants submit that this is an acronym well known to those skilled in the art as "radio frequency." The specification and drawings both support reception of signals in the 950MHz-2150MHz bandwidth which are known to those skilled in the art to be radio frequency, or RF, signals. Paragraphs 2 and 8 of the specification further refer to "radiofrequency" which Applicants would assert clearly supports the claimed "RF" language. Applicants present an amendment to the specification to provide explicit support for "RF" with respect to "radio frequency." If the Examiner wishes, Applicants would accept and Examiner's amendment to replace "RF" in the claim language with "radio frequency."

The claims were rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. This rejection concerns the claim language for "RF" and "digital domain." Applicants respectfully request reconsideration and withdrawal of this Section 112 rejection in view of the comments presented above and the amendments to the specification presented herein.

A. Rejections based on the Tan reference

Claim 1 was rejected under 35 U.S.C. 103(a) as being unpatentable over Tan. Applicants respectfully traverse and request reconsideration.

The Examiner asserts that Tan suggests the claimed "integrated circuit embodied on a single monolithic substrate" which includes "a tuning circuit" and "several channel decoding digital circuits" which "are fabricated on that single monolithic substrate." In support of the Examiner's position, the Examiner points to a teaching in Tan that "The IC is a monolithic mixed signal device [which] incorporates a 10b A/D converter [3], analog phase-locked loops (PLL's), interpolating demodulator, square-root raised cosine receive filters, timing/carrier recovery loops, 20-tap complex equalizer, and a t=8 (204,188) Reed-Solomon forward error correction (FEC) decoder." Page 2205, left column. Applicants respectfully disagree.

Claim 1 recites "a tuning circuit of the direct sampling type including mixed analog and digital circuitry configured to receive ***RF satellite digital television signals***" (emphasis added). This limitation requires that the "tuning circuit" which is "fabricated on that single monolithic substrate" receive radio frequency (RF) signals. The Receiver IC disclosed by Tan DOES NOT receive RF signals.

In support of Applicants' position, Applicants would direct the Examiner's attention to the Abstract of the Tan reference where it states that the "chip accepts an analog 2 Vpp differential QAM signal centered at an ***intermediate frequency***" (emphasis added). Tan Figure 3 shows that the "Receiver IC" receives signals at an intermediate frequency IF_2 that is equal to $F_S/4$. The term "F_S" is the sampling clock frequency (also referred to as "sclk") of, for example, 32 MHz. Page 2205, right column, Section II. Thus, in this example the intermediate frequency IF_2 would be 8MHz. The chip received signals at a frequency of 8MHz are clearly NOT radio frequency (RF) signals in the context of the Tan reference, but rather are simply intermediate frequency (IF) signals.

Tan Figure 3 further emphasizes that intermediate frequency (IF) signals, and not radio frequency (RF) signals, are at the input of the Receiver IC by noting that the input signals to the off-chip "Tuner" are "RF" signals, and further that two different IF signals are present (as a

result of an analog dual conversion operation shown with the off-chip Tuner and downstream off-chip mixer).

Claim 1 further recites "a tuning circuit of the direct sampling type including ***mixed analog and digital circuitry***" (emphasis added). This limitation requires that the "tuning circuit" which is "fabricated on that single monolithic substrate" include both analog and digital circuits (See, Applicants Figure 1 and the tuner TZ). This mixed circuitry for the RF tuner is not present on the Receiver IC (Figure 3) of Tan. Rather, Tan shows the use of IF digital tuning circuitry following A/D conversion. Page 2205, right column, Section II.A. The RF analog tuning functionality in the Tan reference is performed OFF-CHIP by the Tuner and dual conversion intermediate frequency (IF) processing components. Still further, the tuning in Tan on the Receiver IC relates to IF signals and NOT the radio frequency RF signals recited by claim 1.

Claim 1 further recites "a circuit input for ***direct sampling at RF***" (emphasis added) within the tuning circuit. This limitation requires that the "tuning circuit" which is "fabricated on that single monolithic substrate" perform direct sampling at RF with respect to the received signals. This is not taught by Tan. As discussed above, and as is clearly shown in Tan Figure 3, the Receiver IC includes an A/D converter which samples a received signal, BUT that received signal is an intermediate frequency (IF) signal, NOT a radio frequency (RF) signal as claimed. Tan does not teach having the Receiver IC function to direct sample the RF signal.

In view of the forgoing, Applicants respectfully submit that claim 1 is patentable over Tan.

Applicants would further point out that Tan's teaching for separating the digital Receiver IC from the RF analog tuning circuitry teaches away from the claimed invention wherein such mixed analog and digital circuitry is provided on a single substrate.

Claim 9 was rejected under 35 U.S.C. 103(a) as being unpatentable over Tan in view of Tomasz. Applicants respectfully traverse and request reconsideration. Claim 9 is patentable over the cited art for at least the reasons recited above with respect to claim 1. Tomasz does not address the deficiencies noted with respect to Tan.

Claim 2 was rejected under 35 U.S.C. 103(a) as being unpatentable over Tan in view of Tomasz and Robbins. Applicants respectfully traverse and request reconsideration. Claim 2 is

patentable over the cited art for at least the reasons recited above with respect to claim 1. Tomasz and Robbins do not address the deficiencies noted with respect to Tan.

Claim 3 was rejected under 35 U.S.C. 103(a) as being unpatentable over Tan in view of Tomasz and Hwang. Applicants respectfully traverse and request reconsideration. Claim 3 is patentable over the cited art for at least the reasons recited above with respect to claim 1. Tomasz and Hwang do not address the deficiencies noted with respect to Tan.

Claims 4-6 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tan in view of Tomasz, Robbins and Hwang. Applicants respectfully traverse and request reconsideration. Claims 4-6 are patentable over the cited art for at least the reasons recited above with respect to claim 1. Tomasz, Robbins and Hwang do not address the deficiencies noted with respect to Tan. Additionally, the rejection of claim 6 is inconsistent with the Examiner's indication on page 58 of the office action that claim 6 is allowable.

Claims 7-8 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tan in view of Lieber. Applicants respectfully traverse and request reconsideration. Claims 7-8 are patentable over the cited art for at least the reasons recited above with respect to claim 1. Tomasz, Robbins and Hwang do not address the deficiencies noted with respect to Tan.

B. Rejections based on the Tomasz reference

Claims 10, 11, 13-15, 20, 38, 48-50 and 55 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz in view of Robbins.

With respect to claim 10, Applicants previously pointed out that the claim requires that the "circuitry of the converter, tuners and channel decoding digital circuits are fabricated on that single monolithic substrate." The Examiner had referenced Tomasz's preferred embodiment of "a single integrated circuit." It was Applicants' position that this reference to "a single integrated circuit," when taken in proper context, refers only to integrating the tuner functionality on a single substrate. The A/D converter and digital processing circuits are specifically taught by Tomasz to be integrated on separate substrates distinct from the tuner "single integrated circuit." There was no teaching or suggestion for the claimed fabrication of the recited mixed analog and digital circuitry on a single monolithic substrate.

The Examiner apparently agrees with the Applicants that Tomasz fails to teach the claimed "single monolithic substrate" including the recited mixed analog and digital circuitry. It is the Examiner's position, however, that it would be obvious for one skilled in the art to have the "individual modules/circuit components reside as integrated together or as separate parts." See, Final Office Action, page 59. In support, the Examiner cites to In re Larson, 340 F.2 965, 968 (CCPA 1965). Larson, however, clearly notes that the test for obviousness concerns an evaluation of whether there exists ***an obvious engineering choice***. Applicants submit that the integration of ***mixed analog and digital circuitry of the type claimed by Applicants*** on a single substrate is not an obvious engineering choice because the noise of the baseband digital circuitry can have adverse effects on the operation of the RF analog circuitry and common integration of such circuits is not known in the cited prior art. This technical issue is not easy to solve, the prior art typically provided separate substrates, and the Examiner has notably failed to cite to a reference showing mixed analog and digital circuitry of the type claimed by Applicants on a single substrate.

Applicants would additionally point out that the problems associated with mixed analog and digital circuitry of the type claimed by Applicants on a single substrate become more severe when the analog circuitry at issue is handling analog signals at radio frequency (RF). The presence of the baseband digital signal processing circuitry, with its associated noise, makes it more difficult (an engineering challenge) to fabricated mixed analog and digital circuitry on a common substrate with analog RF processing. The prior art of record fails to indicate that an obvious engineering choice exists for providing mixed analog and digital circuitry on a single substrate.

Larson concerned moving from two parts which are mounted together (rigidly secured) to two parts which are integrally formed. The teaching for combining and securing the two parts together existed in the prior art. Integral formation was known in the art. Larson suggests that it would be obvious, given a teaching where the two parts are secured together, to move to a product where the two parts are instead provided as an integral unit. More specifically, that it would be an obvious engineering choice, where integrally forming components was known to engineers, to move from separate but secured together parts to instead being integrally formed

parts. Applicants fail to see how this analysis in Larson is material to evaluating the patentability of the claimed invention.

Unlike the Larson situation, where a teaching for mounting components together existed in the prior art and further providing components in an integral manner existed in the prior art, the Examiner here has failed to provide any indication that it was known and possible in the prior art for mounting the components/circuits of mixed analog and digital type claimed by Applicants together on a single substrate. The Examiner's reliance on the Larson citation is misplaced. There is no basis then for assuming that an obvious engineering choice existed to move from the separate substrate teaching of Tomasz to a full scale integration of the mixed analog and digital components as claimed on a common substrate. In fact, the art, most notably the Tomasz reference relied upon by the Examiner, appears to instead teach away from integration of mixed circuits on a common substrate because Tomasz specifically put the analog circuitry on one substrate and the digital circuitry on another substrate. Applicants own specification noted the existence of prior art like that of Tomasz and further addressed that the present invention, with its single substrate and mixed circuitry, was one inventive concept.

Claim 10, along with claims 11, 13-15, 20, is accordingly patentable over the cited prior art.

Claim 38, along with claims 48-50 and 55, is asserted to be patentable over the cited prior art for at least the same reasons as claim 10.

Claims 16-18 and 51-53 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz in view of Robbins and Hwang. Claims 16-18 and 51-53 are patentable over the cited art for at least the reasons recited above with respect to claims 10 and 38.

Claims 21-28, 30-32, 37, 39 and 40-46 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz in view of Robbins and Young.

With respect to claim 21, Applicants claim a single monolithic substrate in relation to claimed mixed analog and digital circuits. The Examiner relies on Tomasz for the teaching of "a single integrated circuit." As discussed above, this single integrated circuit concerned only the analog circuitry in Tomasz. Applicants further assert that this claim is patentable over the cited art for the reasons recited above with respect to claim 10.

Claims 22-28, 30-32 and 37 are patentable because they depend from claim 21.

Claims 39 and 40-46 are patentable because they depend from claim 38.

Claims 12 and 47 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz in view of Robbins and Dapper. Claims 12 and 47 are patentable over the cited art for at least the reasons recited above with respect to claims 10 and 38.

Claims 19 and 54 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz in view of Robbins and Lieber. Claims 19 and 54 are patentable over the cited art for at least the reasons recited above with respect to claims 10 and 38.

Claim 29 was rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz in view of Robbins, Young and Dapper. Claim 29 is patentable over the cited art for at least the reasons recited above with respect to claim 21.

Claims 33-35 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz in view of Robbins, Young and Hwang. Claims 33 and 35 are patentable over the cited art for at least the reasons recited above with respect to claim 21.

Claim 36 was rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz in view of Robbins, Young and Lieber. Claim 36 is patentable over the cited art for at least the reasons recited above with respect to claim 21.

In view of the foregoing, Applicants respectfully submit that the application is in condition for favorable action and allowance.

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Respectfully submitted,

By /Andre M. Szuwalski/
Andre M. Szuwalski
Registration No.: 35,701
Gardere Wynne Sewell LLP
3000 Thanksgiving Tower
1601 Elm Street
Dallas, Texas 75201
(214) 999-4795
Attorney For Applicants